Instruction manual

DATA I/O

Programming systems for tomorrow...today

PROM PROGRAMMER
Program Card Set
909/919-1226-2

025-1226-2

Rev L Jan 79

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SECTION 1
SPECIFICATIONS

1.1 INTRODUCTION

Data I/O Program Card Sets configure the programmer for the requirements of particular devices. This card set, used with the appropriate socket adapter, will program and read the devices listed in Table 1-1. New applications are developed frequently; therefore, consult the most recent Data I/O Comparison Chart of Programmable Devices to supplement Table 1-1.

Table 1-1. Applications of the Program Card Set

Array Size and Technology	PROM Part Number	Programmed Logic Level	Pinout	Socket Adapter
SIGNETICS				
32x8 FL	82S23	VOH OC	16 PIN	1037
32x8 FL	82S123	VOH TS	16 PIN	1037
256x8 FL	82S114	VOH TS	24 PIN	1096
512x8 FL	82S115	VOH TS	24 PIN	1097
256x4 FL	82S126	VOH OC	16 PIN	1035-1
256x4 FL	82S129	VOH TS	16 PIN	1035-1
512x4 FL	82S130	VOH OC	16 PIN	1035-2
512x4 FL	82S131	VOH TS	16 PIN	1035-2
512x8 FL	82S140	VOH OC	24 PIN	1033-2
512x8 FL	82S141	VOH TS	24 PIN	1033-2
512x8 FL	82S146	VOH OC	20 PIN	1064
512x8 FL	82S147	VOH TS	20 PIN	1064
1024x4 FL	82S136	VOH OC	18 PIN	1039-3
1024x4 FL	82S137	VOH TS	18 PIN	1039-3
1024x8 FL	82S180	VOH OC	24 PIN	1033-3
1024x8 FL	82S181	VOH TS	24 PIN	1033-3
1024x8 FL	82S182	VOH OC	24 PIN	1033-3
1024x8 FL	82S183	VOH TS	24 PIN	1033-3
1024x8 FL	82S2708	VOH TS	24 PIN	1033-3
2048x4 FL	82S184	VOH OC	18 PIN	1039
2048x4 FL	82S185	VOH TS	18 PIN	1039
2048x8 FL	82S190	VOH OC	24 PIN	1033
2048x8 FL	82S191	VOH TS	24 PIN	1033

The Program Card Set includes the parts listed in Figure 1-1. The analog card produces the correct voltages in the proper waveforms for the device to be programmed or read. The digital card controls the sequences of these waveforms.

A Program Card Set for use in a System 17 or 19 Programmer is included in a Programming Pak and designated by a 919- part number. See Figure 1-1 a). A card set shipped alone, for use in a Model 1-5, 7 or 9 Programmer, bears a 909- part number. See Figure 1-1 b).

1.3 CALIBRATOR PROGRAM ADAPTER

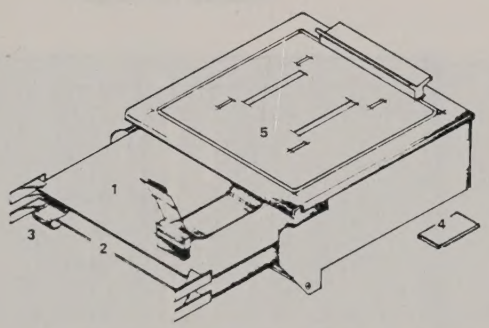
The card set includes a Calibrator Program Adapter which mates with the Data I/O Universal Calibrator (P/N 910-1071). The PROMs on the adapter deliver the control signals to the analog card.

Using the calibrator and following the calibration procedure in Section 4 of this manual, Data I/O customers can be sure the Program Card Set remains within voltage and timing tolerances for effective programming.

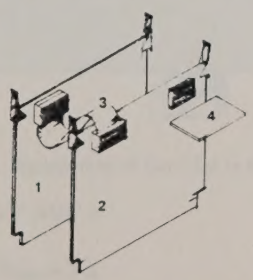
1.4 CALIBRATION REQUIREMENTS

The need for calibration varies with the amount of use; calibration is recommended every ninety days of regular use or if programming yields fall below manufacturer's recommended minimums.

Complete calibration must be performed with a programmer that has an address and data display. Card sets for use in a Model 7 or System 17 may be properly calibrated using another Data I/O programmer. Alternately, Data I/O provides calibration service at regional Service Centers.



a) Programming Pak for System 17 and 19 Programmers



b) Program Card Set for Model 1 - 9 Programmers

1. DIGITAL CARD	701-1225
2. ANALOG CARD	701-1226-2
3. INTERCONNECT CABLE	709-1608
4. CALIB. PROGRAM ADAPTER	910-1226-2
5. PROGRAMMING PAK CARRIER	940-0919

Figure 1-1. Parts included in the a) Programming Pak b) Program Card Set

SECTION 2
INSTALLATION

2.1 DIGITAL CARD JUMPERS

Figure 2-1 shows the customer-selectable-jumper locations on the digital card. Refer to Table 2-1 to check the jumper positions. If a jumper change is ever made, be sure to replace the jumpers in the normal position before using the card set for programming.

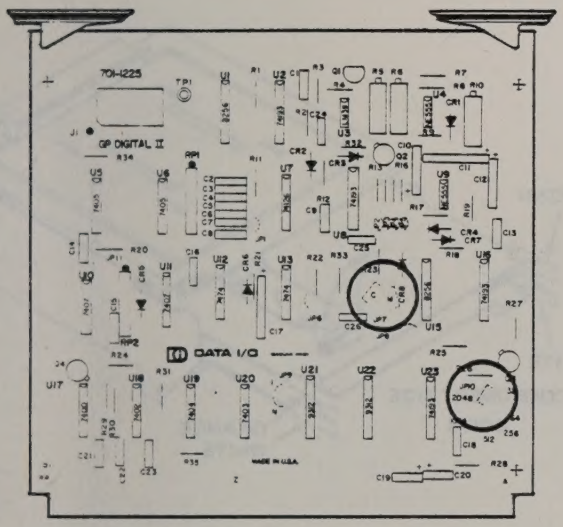


Figure 2-1. Digital Card Jumper Locations

Table 2-1. Customer - Selectable Digital Card Jumpers

JUMPER	FUNCTION	NORMAL POSITION	COMMENTS
JP 7	Reject	C	–
JP 10	Word Limit	2048	–

2.2 CARD SET INSERTION

When changing card sets in Model 1-9 Programmers, turn power OFF.

Power may remain ON when changing Programming Paks in System 17 or 19 Programmers. In this way, data may be retained in RAM during the operation.

2.2.1 MODELS 1-5

Refer to Figure 2-2.

Remove the top cover from the programmer. Each card in the card cage has color-coded extractors which correspond to the colors of the card guides. Install the analog card in the white/white position in the card cage. Install the digital card in the front brown/orange position. Components of both cards must face forward in Model 3 and 5 Programmers and to the right in Model 1 Programmers. Insert the cable into the socket receptacle, route it over the card cage, and attach it to J2 on the analog card. Be sure the cable is oriented correctly: the red stripe must align with the connector dot.

CAUTION

Installing the cable backwards could cause programmer damage.

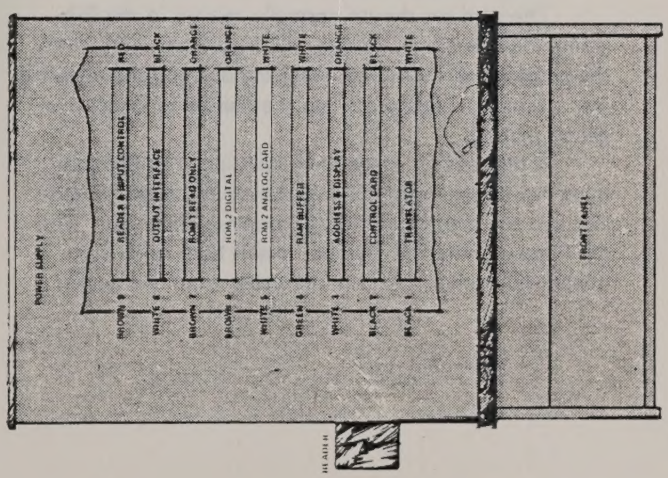


Figure 2-2. Installation of Card Set in Model 3 or 5

2.2.2 MODELS 7 AND 9

Refer to Figure 2-3.

The card set access door is located at the front of the programmer on the right-hand side. Open the door from the bottom to expose the card slots. The card guides are colored white/white and brown/orange to correspond with the extractor tabs on the cards. Insert both cards component-side-down – the analog card in the white/white slot and the digital in the brown/orange. Attach the cable from the socket receptacle to connector J2 on the analog card. Be sure the cable is oriented correctly: the red stripe must align with the connector dot.

CAUTION

Installing the cable backwards could cause programmer damage.

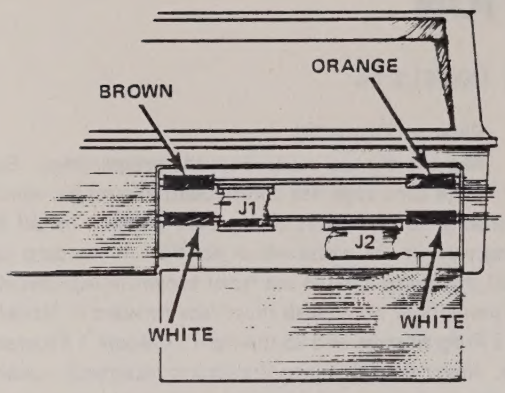


Figure 2-3. Installation of Card Set in Model 7 or 9

2.2.3 SYSTEMS 17 AND 19

Refer to Figure 2-4.

The card set should normally remain in the Programming Pak frame. Install the Programming Pak into the programmer by sliding it into the opening and lowering into position. Press gently on the handle to insure connector mating.

If the card set needs to be installed in its Programming Pak frame, insert the analog card in the white/white slot and the digital card in the brown/orange slot. With the Programming Pak face up, install both cards component-side-down. Attach the cable from the socket receptacle to connector J2 on the analog card. Be sure the cable is oriented correctly: the red stripe must align with the connector dot.

CAUTION

Installing the cable backwards could cause programmer damage.

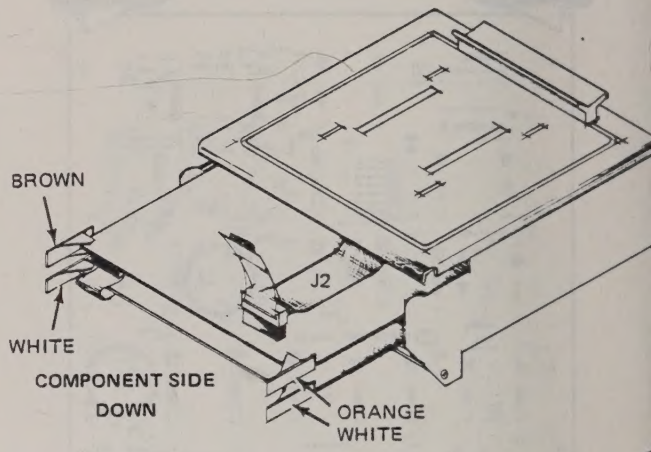


Figure 2-4. Installation of the Program Card Set in the Programming Pak

SECTION 3
OPERATION

The Program Card Set provides the link between the device in the socket adapter and the programmer's memory and control electronics. Its functions are directly controlled by the programmer. Complete instructions for operations using the card set are in the programmer instruction manual.

SECTION 4

CALIBRATION

4.1 INTRODUCTION

Calibration includes checks of power supply levels, steady-state tests of critical programming parameters, and verification of resistively loaded programming waveforms. The need for calibration varies with the amount of use, but calibration is suggested at least every ninety days. For calibration by the customer, the procedure in this section should be followed in sequence.

NOTE

If any adjustment is necessary, complete the entire calibration procedure.

4.2 TEST SET-UP

The following equipment is required to perform a calibration:

1. Data I/O Universal Calibrator, P/N 910-1071
2. Calibrator Extender Fixture:

Models 1-5	P/N 910-1136
Model 9	P/N 910-1074
System 19	P/N 910-1520

3. Digital voltmeter (DVM) — Fluke Model 8000A or equivalent.
4. A potentiometer adjustment tool
5. Dual-trace oscilloscope — Tektronix 465 or equivalent
6. A jumper wire approximately 12 inches in length
7. Data I/O interconnection cables:
   Models 1-5: P/N 709-1613
   Model 9, System 19: P/N 709-2608, 709-1613.
8. Calibrator Program Adapter

To prepare for calibration of the programmer power supplies and the Program Card Set, remove the card set from the programmer and connect the Universal Calibrator according to the following instructions:

4.2.1 MODELS 1 — 5

Refer to Figure 4-1.

1. Make sure the programmer power is OFF.
2. Remove the cover from the programmer and remove the Program Card Set from the card cage.
3. Disconnect the 16-conductor cable from J1 on the digital card; disconnect the 26-conductor cable from J2 on the digital card.

CAUTION

Connector pins are fragile; use a suitable tool, such as a small screwdriver, when removing cables from their connectors.

4. Install the Extender Card, P/N 910-1136, (with the Universal Calibrator attached) into the programmer's analog card position (white/white). Be sure that the edge of the Extender Card is securely seated. Reinstall the digital card in the digital card position (brown/orange) in the programmer card cage.
5. Connect the 16-conductor cable from J1 on the analog card to J1 on the Universal Calibrator. Connect the 26-conductor cable from J2 on the analog card to J2 on the Universal Calibrator. Be sure the cables are oriented correctly: the red stripes must align with the connector dots.
6. Plug the Calibrator Program Adapter into the Program Adapter socket on the Universal Calibrator.

CAUTION

Be sure the 910-XXXX part number corresponds to the 909-XXXX part number of the Program Card Set.

7. Connect the DVM ground lead to the GND test point on the Universal Calibrator.
8. Turn the programmer power ON. Prepare the programmer for calibration using the following key sequence:

   RESET
   ROM2 — ROM2
   MANUAL
   PROGRAM
   START

4.2.2 MODEL 9

Refer to Figure 4-2.

1. Make sure the programmer power is OFF.
2. Open the Program Card Set access door from the bottom. Remove the Program Card Set.

Figure 4-1. Set-up of Models 1-5 for DC Calibration

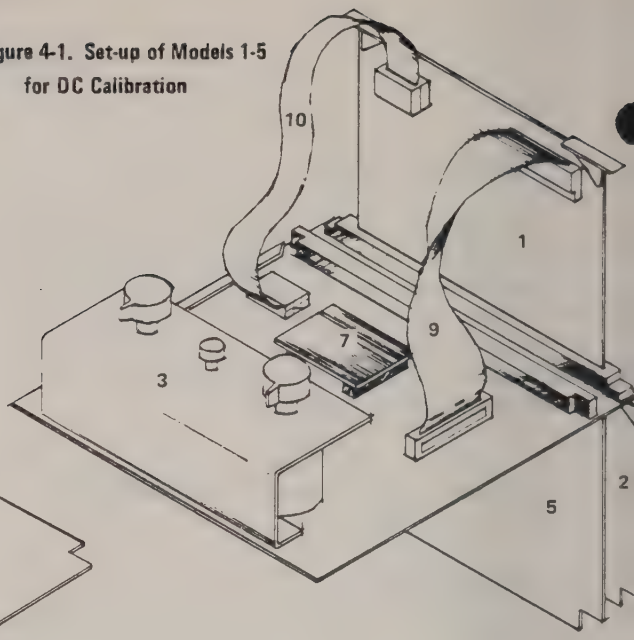
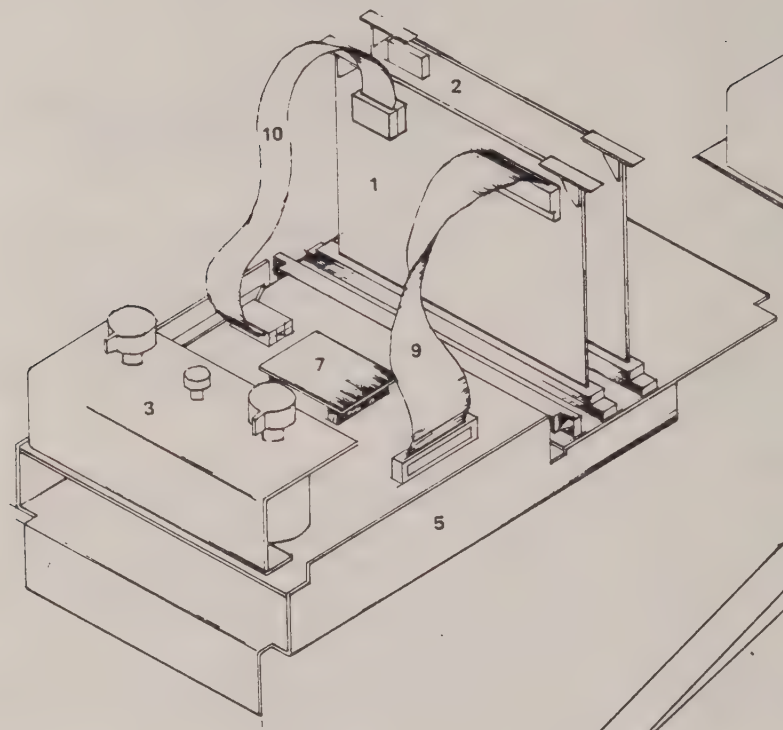


Figure 4-2. Set-up of Model 9 for DC Calibration



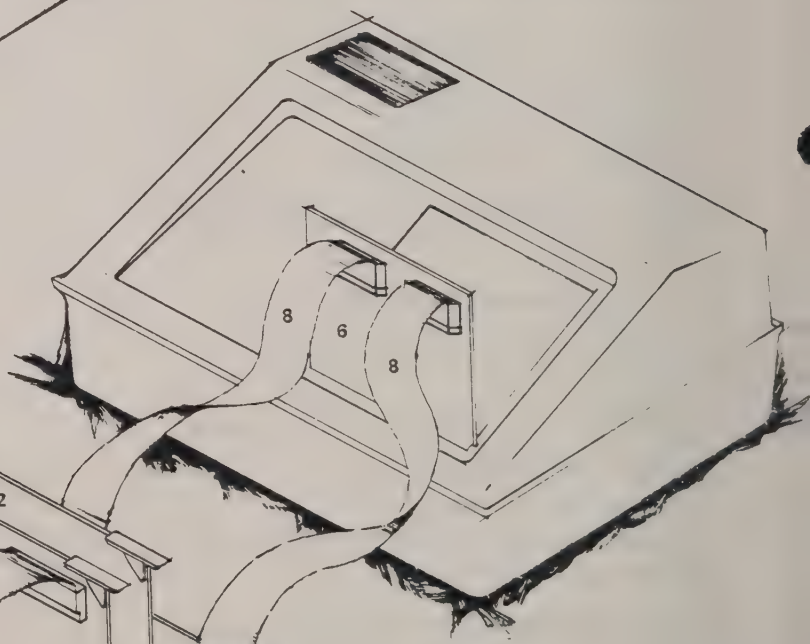
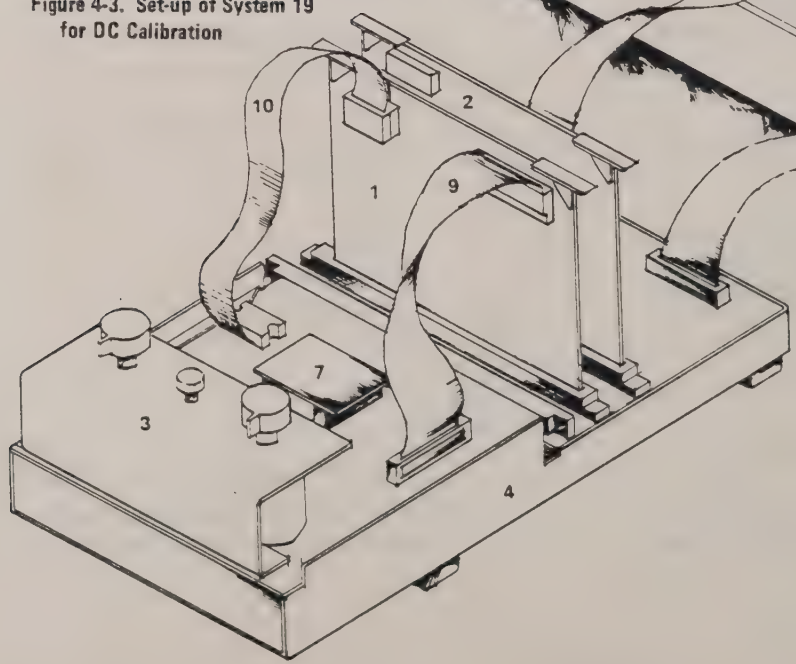


Figure 4-3. Set-up of System 19 for DC Calibration



1. ANALOG CARD
2. DIGITAL CARD
3. UNIVERSAL CALIBRATOR
4. CALIBRATOR EXTENDER
5. CALIBRATOR EXTENDER FIXTURE
6. CALIBRATOR INTERFACE
7. CALIBRATOR PROGRAM ADAPTER
8. 50-CONDUCTOR CABLE
9. 26-CONDUCTOR CABLE
10. 16-CONDUCTOR CABLE

CAUTION

Connector pins are fragile; use a suitable tool, such as a small screwdriver, when removing cables from their connectors.

3. Disconnect the 16-conductor cable from J1 on the digital card; disconnect the 26-conductor cable from J2 on the digital card.

4. Install the Extender Card, P/N 910-1074, (with the Universal Calibrator attached) into the programmer's analog card position (white/white). Be sure that the edge of the Extender Card is securely seated. Reinstall the digital card into the digital card position (brown/orange) in the programmer card cage.

5. Connect the 16-conductor cable from J1 on the analog card to J1 on the Universal Calibrator. Be sure the cables are oriented correctly: the red stripes must align with the connector dots.

6. Plug the Calibrator Program Adapter into the Program Adapter socket on the Universal Calibrator.

CAUTION

Be sure the 910-XXXX part number corresponds to the 909-XXXX part number of the Program Card Set.

7. Connect the DVM ground lead to the GND test point on the Universal Calibrator.

8. Turn the programmer power ON. Prepare the programmer for calibration using the following key sequence:

   EXECUTE

   NORMAL/INVERT switch to INVERT

4.2.3 SYSTEM 19

Refer to Figure 4-3.

1. Make sure the programmer is OFF.

2. Remove the Programming Pak from the programmer.

3. Insert the Calibrator Interface, P/N 702-1538, into the Programming Pak port.

4. Connect the two 50-pin cables, P/N 709-2700, to the Calibrator Interface card. Be sure the cables are oriented properly: the red stripes must align with the connector dots.

5. Connect the free ends of the 50-pin cables to the Universal Calibrator/Calibrator Extender Fixture. Be sure the cables are oriented with the red stripes and connector dots aligned.

6. Remove the card set to be calibrated from its Programming Pak by disconnecting J2 of the analog card from the Programming Pak socket receptacle PC board.

7. Install the card set in the two blue card slots on the Calibrator Extender. The analog card should be in front with the component sides of both boards facing the Universal Calibrator.

8. Connect the 26-conductor cable from J2 of the analog card to J2 of the Universal Calibrator, making sure to align the red stripe to the connector dot.

9. Disconnect the 16-conductor cable from J1 on the digital card and route it to J1 on the Universal Calibrator, making sure to align the red stripe to the connector dot.

10. Plug the Calibrator Program Adapter into the Program Adapter socket on the Universal Calibrator.

CAUTION

Be sure the 910-XXXX part number of the Calibrator Program Adapter corresponds to the 909-XXXX part number of the Program Card Set.

11. Connect the DVM ground lead to the GND test point on the Universal Calibrator.

12. Turn the programmer power ON. Prepare the programmer for calibration using the following key sequence:

    SELECT
    C1
    START

    The TEST light will come ON.

4.3 PROCEDURES FOR CALIBRATION

The Calibration Chart, between pages 4-4 and 4-5, gives the steps for complete DC calibration. It is to be used only with the Calibrator Program Adapter specified in the title block of the chart.

The first five steps on the Calibration Chart cover the level checks of the programmer power supplies. If any adjustment is necessary in these steps, refer to the Programmer Manual. The remaining steps provide information for calibration of the Program Card Set.

● The PROGRAMMER WORD COUNT column is divided into three portions: DEC (Decimal), HEX (Hexadecimal), and OCT (Octal). When performing each step, set the address (word count) corresponding to the address number base of the programmer in use. For instance, with a programmer having a hexadecimal address readout, ignore the DEC and OCT columns.

CAUTION

DO NOT leave Word Count (address) advanced beyond 000 for extended periods. Static conditions created by the Universal Calibrator may cause thermal damage to components if the programmer is left unattended with advanced word count.

● The TEST DESCRIPTION column specifies the function to be checked in each step. In most cases, the steps simply require a DVM reading to insure that a level is within tolerance. Some steps, labeled Adjustment Steps, give a nominal (NOM) value and prescribe adjustment to that value if the level is out of the MIN-MAX range.

● The ADJUSTMENT column calls out potentiometer designations. The first four entries in the ADJ column refer to power supply potentiometers located on the power supply board of the programmer. The remaining entries in the ADJ column refer to potentiometers on the analog card. Refer to Figure 4-4 for locations of the potentiometers.

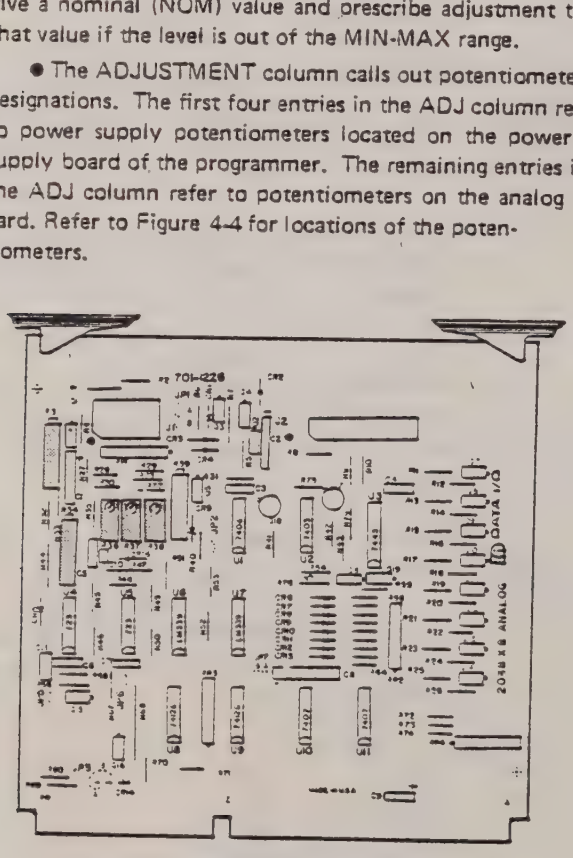


Figure 4-4. Analog Card Adjustment Locations

● The SWITCH POSITIONS column gives the switch settings for S2 and S3 on the Universal Calibrator. S2 is the load-select switch; S3 is the line-select switch. Each step on the calibration chart may require changing of switch positions. With the proper S2 and S3 positions selected, press S1 to make an accurate reading, and keep the switch depressed only long enough to complete the step.

CAUTION

DO NOT keep S1 depressed for extended periods. Certain measurements induce high programmer current levels. Extended high-current operation (S1 depressed) may damage sensitive electronic components.

● The TEST POINT column gives test point locatio for the DVM probe. Most test points are located on th Universal Calibrator; some points are located on the p gram card. For instance, if a test point is designated U6 P8, the DVM probe should be placed on pin 8 of integrated circuit U6 on the card indicated in the COMMENTS column.

● The LIMITS column is divided into three portion MIN (minimum), NOM (nominal), and MAX (maximum The values given are in volts and indicate the range int which a given DVM reading should fall. If a reading is within the limits, no adjustment is required and the pr grammer (or Program Card Set) passes a particular test If a reading falls outside of the given limits, or if it cannc be adjusted to fall within the limits (in adjustment steps) the card is nonfunctional and should not be used for pro gramming.

● The COMMENTS column on the right side of the chart provides information for certain calibration step including call-outs of programmer operations required i some steps. The programmer provides signals to the carc set on the Address bus, the Data Input bus, the START/ STOP line and the FWD/REV line. The card set provides signals to the programmer on the RESET line, the VOL/ VOH select line and the Data Output bus. In the course of calibration, the programmer is used to observe or set following conditions:

- State of the START/STOP line
- State of the FWD/REV line
- Data on the DO bus
- Data on the DI bus

Key sequences for observing these conditions are given in the following paragraphs (4 3.1 – 4.3.5). Follow the tests on the Calibration Chart step-by-step, and refer paragraphs 4.3.1 – 4.3.5 as necessary.

MODEL 9 USERS NOTE

Some of the following operations are performed differently on Model 9's with different revisions o software. Perform the following test to determine whether to refer to steps for Revision "A" software or to steps for Revision "B" or later software.

1. *Turn power OFF.*
2. *Observe the LOAD indicator while turning power ON.*
3. *If the LOAD indicator remains ON, refer to key sequences for Revision "B" or later software.*
4. *If the LOAD indicator turns OFF, refer to key sequences for Revision "A" software.*

Calibration Chart

DATA I/O
Programming systems for tomorrow...today

CALIBRATION CHART 017-1226-2 | PROGRAM CARD 909-1226-2
FIXTURE 702-1071 | MANUFACTURER SIGNETICS
PAGE 1 OF 2 | PROGRAM ADAPTER 910-1226-2 | PROM SIG. GENERIC FAMILY

DATE	REV	REVISION RECORD	DR	CK
2-24-78	E	C.N. #2125	KL	KJ
3-78	-	Update Pg 3-3	KM	ME
8-78	F	C.N. #2406	KJ	DB
11-78	-	C.N.#2565 (re-typed)	FS	

CAL. ADAPT. HEX DATA (POS. LOGIC) LOCATION U2	U1	TEST DESCRIPTION	STEP NO.	PROGRAMMER WORD COUNT DEC	HEX	OCT	SWITCH POSITIONS S2	S3	MEASUREMENT TEST PT.	ADJ.	LIMITS MIN	NOM	MAX
64	00	+24	1-1	000	00	000			+24	R26	23.5	24.0	24.5
64	00	FIXED +48	1-2	000	00	000			+48	R24	49.4	49.7	49.8
64	00	SUPPLIES + 5	1-3	000	00	000			+ 5	R18	5.05	5.1	5.15
64	00	- 9	1-4	000	00	000			-9	R40	-9.2	-9.0	-8.8
64	00	PROGRAMMABLE SUPPLY	1-5	000	00	000			PROG V		11.75		13.75
64	00	VCC VERIFY, FWD	2-1	001	01	001	5	1	TP3	R36	4.4	4.5	4.6
64	04	VCC PROGRAM V SET (1)	2-2	002	02	002	5	1	TP3	R37	8.50	8.75	9.00
64	00	VCC VERIFY, REV	2-3	001	01	001	5	1	TP3	R38	5.4	5.5	5.6
44	00	VCC KILL	2-4	003	03	003	5	1	TP3		0.0		0.4
64	01	VERIFY LOGIC	3-1	004	04	004	7	5	U6 P8		1.4		1.7
64	01	$\overline{CE2}$ LOW	4-1	004	04	004	10	5	TP3		0.0		0.4
64	00	$\overline{CE2}$ HIGH (2)	4-2	005	05	005	7	5	TP3		4.8		5.15
64	E6	BIT 8 PROGRAM V OUT SET	5-1	006	06	006	3	8	TP3	R34	16.5	17.0	17.5
64	C6	BIT 8 DESELECT	5-2	007	07	007	2	8	TP3		4.0		4.8
64	C6	BIT 7 PROGRAM V OUT SET	5-3	007	07	007	3	9	TP3		16.5		17.5
64	A6	BIT 7 DESELECT	5-4	008	08	010	2	9	TP3		4.0		4.8
64	A6	BIT 6 PROGRAM V OUT SET	5-5	008	08	010	3	10	TP3		16.5		17.5
64	86	BIT 6 DESELECT	5-6	009	09	011	2	10	TP3		4.0		4.8
64	86	BIT 5 PROGRAM V OUT SET	5-7	009	09	011	3	11	TP3		16.5		17.5
64	66	BIT 5 DESELECT	5-8	010	0A	012	2	11	TP3		4.0		4.8
64	66	BIT 4 PROGRAM V OUT SET	5-9	010	0A	012	3	12	TP3		16.5		17.5
64	46	BIT 4 DESELECT	5-10	011	0B	013	2	12	TP3		4.0		4.8
64	46	BIT 3 PROGRAM V OUT SET	5-11	011	0B	013	3	23	TP3		16.5		17.5
64	26	BIT 3 DESELECT	5-12	012	0C	014	2	23	TP3		4.0		4.8
64	26	BIT 2 PROGRAM V OUT SET	5-13	012	0C	014	3	22	TP3		16.5		17.5
64	06	BIT 2 DESELECT (4)	5-14	013	0D	015	2	22	TP3		4.0		4.8
64	06	BIT 1 PROGRAM V OUT SET (3)	5-15	013	0D	015	3	21	TP3		16.5		17.5
64	E6	BIT 1 DESELECT	5-16	014	0E	016	2	21	TP3		4.0		4.8

COMMENTS - Use paragraphs 4.3.1 - 4.3.5 for key sequences for comments below.
Switch S1 must be depressed for accurate readings.
CAUTION: DO NOT LEAVE S1 DEPRESSED FOR EXTENDED PERIODS.

See NOTE 1, on page 2.
Adjustments are located on the power supply board.
See programmer manual.

Set programmer in FWD. *Adjustment Step.*

Adjustment Step.

Set programmer in REV. *Adjustment Step.*

Test point located on analog card.

Adjustment Step.

CAL. ADAPT. HEX DATA (POS LOGIC) LOCATION U2	U1	TEST DESCRIPTION	STEP NO.	PROGRAMMER WORD COUNT DEC	HEX	OCT	SWITCH POSITIONS S2	S3	MEASUREMENT TEST PT.	ADJ.	LIMITS MIN	NOM	MAX
E4	00	BIT 8 COMPARATOR	6-1	015	0F	017	3	8					
E4	00	BIT 7 COMPARATOR	6-2	015	0F	017	3	9					
E4	00	BIT 6 COMPARATOR	6-3	015	0F	017	3	10					
E4	00	BIT 5 COMPARATOR	6-4	015	0F	017	3	11					
E4	00	BIT 4 COMPARATOR	6-5	015	0F	017	3	12					
E4	00	BIT 3 COMPARATOR	6-6	015	0F	017	3	23					
E4	00	BIT 2 COMPARATOR	6-7	015	0F	017	3	22					
E4	00	BIT 1 COMPARATOR	6-8	015	0F	017	3	21					
64	66	ADDRESS TEST A0 VIL (5)	7-1	682	2AA	1252	7	20	TP3		0.0		0.4
64	66	ADDRESS TEST A1 VIH	7-2	682	2AA	1252	7	19	TP3		4.8		5.15
64	66	ADDRESS TEST A2 VIL	7-3	682	2AA	1252	7	18	TP3		0.0		0.4
64	66	ADDRESS TEST A3 VIH	7-4	682	2AA	1252	7	17	TP3		4.8		5.15
64	66	ADDRESS TEST A4 VIL	7-5	682	2AA	1252	7	16	TP3		0.0		0.4
64	66	ADDRESS TEST A5 VIH	7-6	682	2AA	1252	7	15	TP3		4.8		5.15
64	66	ADDRESS TEST A6 VIL	7-7	682	2AA	1252	7	14	TP3		0.0		0.4
64	66	ADDRESS TEST A7 VIH	7-8	682	2AA	1252	7	13	TP3		4.8		5.15
64	66	ADDRESS TEST A8 VIL	7-9	682	2AA	1252	7	2	TP3		0.0		0.4
64	66	ADDRESS TEST A9 VIH	7-10	682	2AA	1252	7	3	TP3		4.8		5.15
64	66	ADDRESS TEST A10 VIL	7-11	682	2AA	1252	7	4	TP3		0.0		0.4
64	00	ADDRESS TEST A0 VIH	7-12	1365	555	2525	7	20	TP3		4.8		5.15
64	00	ADDRESS TEST A1 VIL	7-13	1365	555	2525	7	19	TP3		0.0		0.4
64	00	ADDRESS TEST A2 VIH	7-14	1365	555	2525	7	18	TP3		4.8		5.15
64	00	ADDRESS TEST A3 VIL	7-15	1365	555	2525	7	17	TP3		0.0		0.4
64	00	ADDRESS TEST A4 VIH	7-16	1365	555	2525	7	16	TP3		4.8		5.15
64	00	ADDRESS TEST A5 VIL	7-17	1365	555	2525	7	15	TP3		0.0		0.4
64	00	ADDRESS TEST A6 VIH	7-18	1365	555	2525	7	14	TP3		4.8		5.15
64	00	ADDRESS TEST A7 VIL	7-19	1365	555	2525	7	13	TP3		0.0		0.4
64	00	ADDRESS TEST A8 VIH	7-20	1365	555	2525	7	2	TP3		4.8		5.15
64	00	ADDRESS TEST A9 VIL	7-21	1365	555	2525	7	3	TP3		0.0		0.4
64	00	ADDRESS TEST A10 VIH	7-22	1365	555	2525	7	4	TP3		4.8		5.15
64	00	GROUND TEST	8-1	1365	555	2525	8	24	TP3		0.0		0.08
64	00	← DATA PATTERN FOR ALL WORDS NOT SHOWN											

CALIBRATION CHART 017-1226-2

PAGE 2 OF 2

Confirm bits 1 - 7 ON (HEX 7F) on DO Bus.
Confirm bits 1 - 6 & 8 ON (HEX BF) on DO Bus.
Confirm bits 1 - 5, 7 & 8 ON (HEX DF) on DO Bus.
Confirm bits 1 - 4 & 6 - 8 ON (HEX EF) on DO Bus.
Confirm bits 1 - 3 & 5 - 8 ON (HEX F7) on DO Bus.
Confirm bits 1, 2 & 4 - 8 ON (HEX FB) on DO Bus.
Confirm bits 1 & 3-8 ON (HEX FD) on DO Bus.
Confirm bits 2 - 8 ON (HEX FE) on DO Bus.

NOTES: 1. For the System 19, the limits for this test are 0.1 volt below the value specified.

4.3.1 CHECK THE STATE OF THE START/STOP LINE

For steps that require confirmation of the state of the START/STOP line, perform the check as follows. To continue testing after confirming a STOP condition, START the programmer according to paragraph 4.3.2.

Models 1, 2, 3 and 5: Observe the START and STOP indicators.

Model 9: Press the PROM key and observe the data display. The programmer is in STOP if the display is blank; in START if the display shows data.

System 19: Observe the START light.

4.3.2 SET THE STATE OF THE START/STOP LINE

To set the state of the START/STOP line:

Models 1, 2, 3 and 5: Press the START/STOP key.

Model 9: Press KEYBOARD to STOP; press EXECUTE to START.

System 19: To set the START line high, with KEYBD selected and address and data displayed, depress the START key. Reselect KEYBD to STOP.

4.3.3 SET THE STATE OF THE FWD/REV LINE

To set the programmer in FORWARD or in REVERSE:

Models 1, 2, 3 and 5: Press the FWD key or the REV key.

Model 9: See MODEL 9 USERS NOTE, paragraph 4.3, to determine the right revision letter.

Revision "A" Software: Halt the programmer in FWD and in REV by entering data at an address and causing a mis-verify:

1. Ground J1-16 on the analog card.
2. Press LOAD.
3. Press EXECUTE.
4. Press KEYBOARD.
5. Key in data – 01 hex – at address 001.
6. Press VERIFY.
7. Press EXECUTE. The programmer will mis-verify at the address containing data and will STOP in FWD.
8. Press SKIP. The programmer will mis-verify at the address containing data and will halt in REV.

Revision "B" or later Software: Press the FWD key to set the programmer in FORWARD and the REV key to set it in REVERSE.

System 19: With KEYBD selected, press ENTER to set the programmer in FORWARD and REVIEW to set it in REVERSE.

4.3.4 LOAD DATA ONTO THE DI BUS

The data on the calibration chart is to be loaded on the DI bus using the programmer keyboard.

Models 1, 2 and 5: Key in binary data called out on the Calibration Chart. (Bits called out must be ON, bits not called out must be OFF.) Perform the necessary number-system conversions if using an octal or hexadecimal keyboard. Confirm correct data by checking the binary DI display.

Model 3: Use an external source, such as a paper tape reader, to put binary data on the DI bus.

Model 9: (See MODEL 9 USERS NOTE, paragraph 4.3, to determine the correct revision letter.) When using a Model 9, always key in the hex data in parentheses to be sure that the correct data is placed on the DI bus.

Revision "A" Software:

Halt the programmer in the automatic program mode with data on the DI bus.

1. Clear RAM: Select INVERT. Then press and hold the EDIT key while pressing LOAD.
2. Press the KEYBOARD key, and key in hex data called out in parentheses on the calibration chart.
3. Press the PROGRAM key.
4. Ground J1-16 on the analog card.
5. Press EXECUTE and wait for the programmer to abort.
6. Press STOP, KEYBOARD and EXECUTE.
7. Disconnect J1-16 from ground.
8. SET the address specified on the calibration chart in order to make the measurement.

Revision "B" or later Software:

1. With the EXECUTE indicator illuminated and all the others OFF, use the hex keypad to key in hex data called out in parentheses on the calibration chart.

System 19:

Key the hex data in parentheses into RAM at the specified address. The data and address shown in the display are present on the DI bus.

4.3.5 CONFIRM DATA ON THE DO BUS

To view DO Bus data:

Models 1, 2, 3 and 5: Compare the bit callout on the calibration chart with the OUTPUT DATA display on the programmer front panel. Bits not called out must be OFF.

Model 9: Press the PROM key and observe the data display on the programmer front panel. Data must match the hex callouts on the calibration chart.

System 19: With KEYBD selected, press the DEVICE DATA key.

4.4 WAVEFORM OBSERVATION

Programming waveforms should be observed after complete DC calibration of the programmer and Program Card Set. Set-up instructions assume that the calibration equipment is already installed for calibration per paragraph 4.2.

In waveform observation, oscilloscope displays are to be compared with the Timing Diagram. These waveforms, indicated by circled digits on the timing diagram, are indentically referenced on the Calibration Chart. Waveforms are selected using switches S2 and S3 on the Universal Calibrator as specified on the Calibration Chart.

4.4.1 CALIBRATION EQUIPMENT SET-UP

Refer to Figure 4-5.

1. Make sure that the programmer power is OFF.
2. Remove the digital card from the card slot.
3. Check the timing diagram to determine the number of the reject jumper. Find and remove the jumper on the digital card (if installed), making sure to note the position in which it is installed.

CAUTION

Be sure to replace the reject (abort) jumper (if it was installed) in the proper position after waveform observation.

4. Disconnect the 16-conductor cable at J1 of the Universal Calibrator.
5. Connect the free end of the 16-conductor cable to digital card J1, making sure that the red cable stripe and pin 1 are properly oriented.
6. Connect the triggered input of a dual-trace oscilloscope to the digital-card test point as indicated to the left of the TEST waveform on the timing diagram. Connect an input probe to TP3 on the calibrator.
7. Reinstall the digital card in the slot from which it was removed.

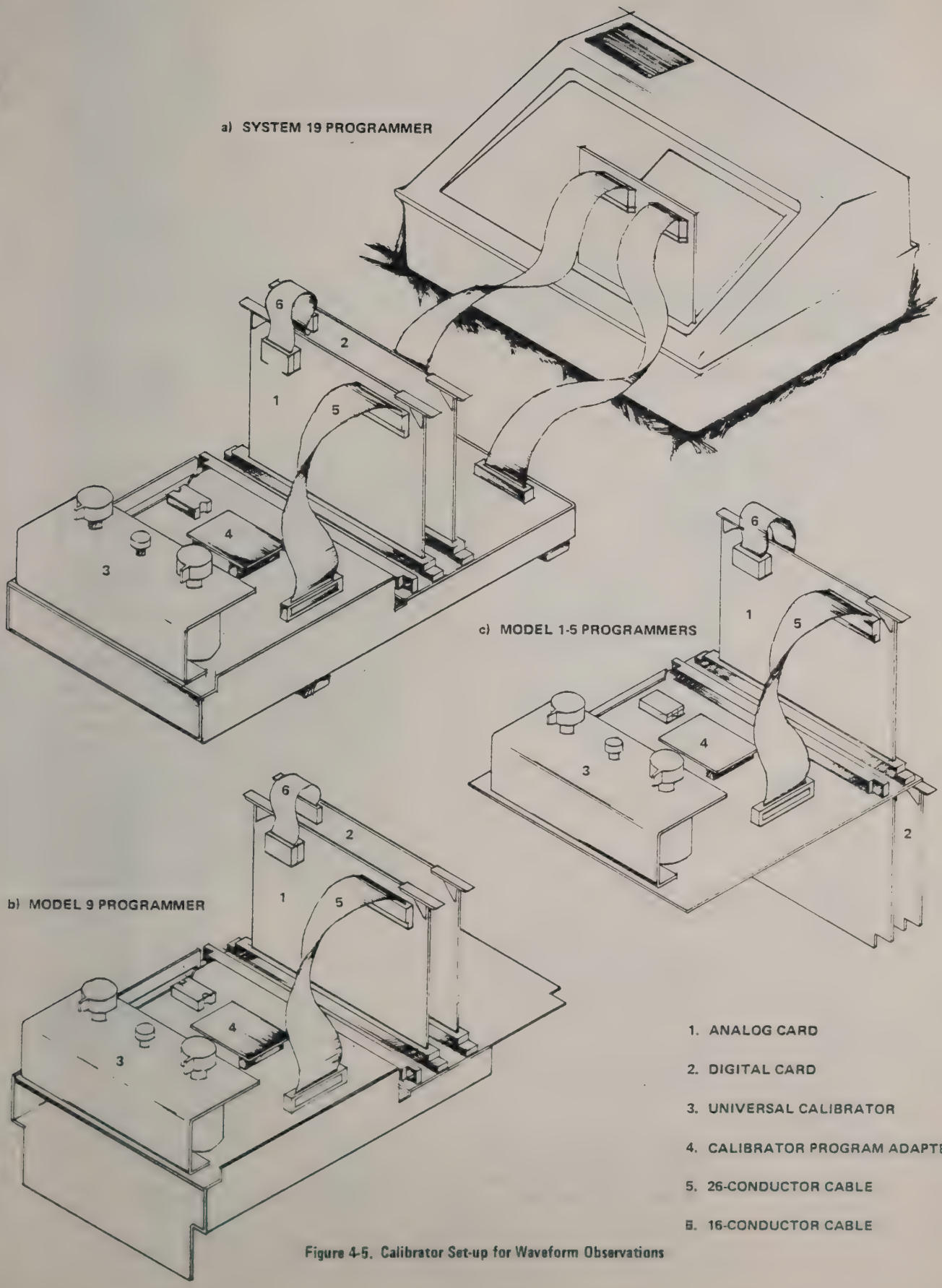


Figure 4-5. Calibrator Set-up for Waveform Observations

8. Check the NOTES column of the timing diagram to determine whether the Program Card Set defaults to VOH or VOL for calibration. If and only if the card set defaults to VOH, ground J1-16 (Read Enable line) to the GND test point on the Universal Calibrator.

CAUTION

Do not connect J1-16 to any other potential; damage to programmer components may result.

4.4.2 TEST PROCEDURE

Observing programming waveforms requires putting data in RAM and causing the programmer to attempt to program a nonexistent device.

1. Turn programmer power ON.

2. Prepare the programmer for keyboard data entry.

Models 1 – 5, press: RESET
RAM-RAM
PROGRAM
MANUAL
START

Model 9: Set the NORMAL/INVERT switch in NORMAL if the Program Card Set is calibrated VOH or in the INVERT position if VOL. The NOTES column on the timing diagram specifies the correct polarity. Press: KEYBOARD.

System 19 press: KEYBD
Ø
ENTER

3. Key in data for bit 1 at several addresses:

Models 1 – 5: Enter bit 1 at several addresses and confirm that bit 1 is ON and all other bits are OFF on the DI display.

Model 9: Enter hex data "Ø1" at several addresses.

System 19: Enter hex data at several addresses. Check the NOTES column on the Timing Diagram to determine the correct data polarity. If the timing diagram indicates VOH, enter a hex "1". If the timing diagram indicates VOL, enter a hex "E" for 4-bit card sets; "FE" for 8-bit card sets.

4. Select the PROGRAM mode:

Models 1 – 5, press: RESET
PROGRAM
AUTO
RAM-ROM2

Model 9, press: PROGRAM

System 19, press: SELECT
CØ
START
PROG

5. Initiate waveforms:

Models 1 – 5, press: START

Model 9, press: EXECUTE

System 19, press: START

After initiating the programming sequence, the programmer will halt at the first address which has data. Refer to the timing diagram and calibration chart by the circled digits (①, ②, ③,...). Make the indicated switch selections with S2 and S3 on the Universal Calibrator.

Observe specific waveforms relative to the triggered test pulse by pressing S1 on the calibrator. S3 is used to route analog card output to TP3 (the oscilloscope probe); S2 selects resistive loads that are applied when S1 is pressed. All other information on the calibration charts is of no importance during waveform observation.

CAUTION

When S1 is depressed high currents are induced within the programmer; do not hold S1 depressed for extended periods.

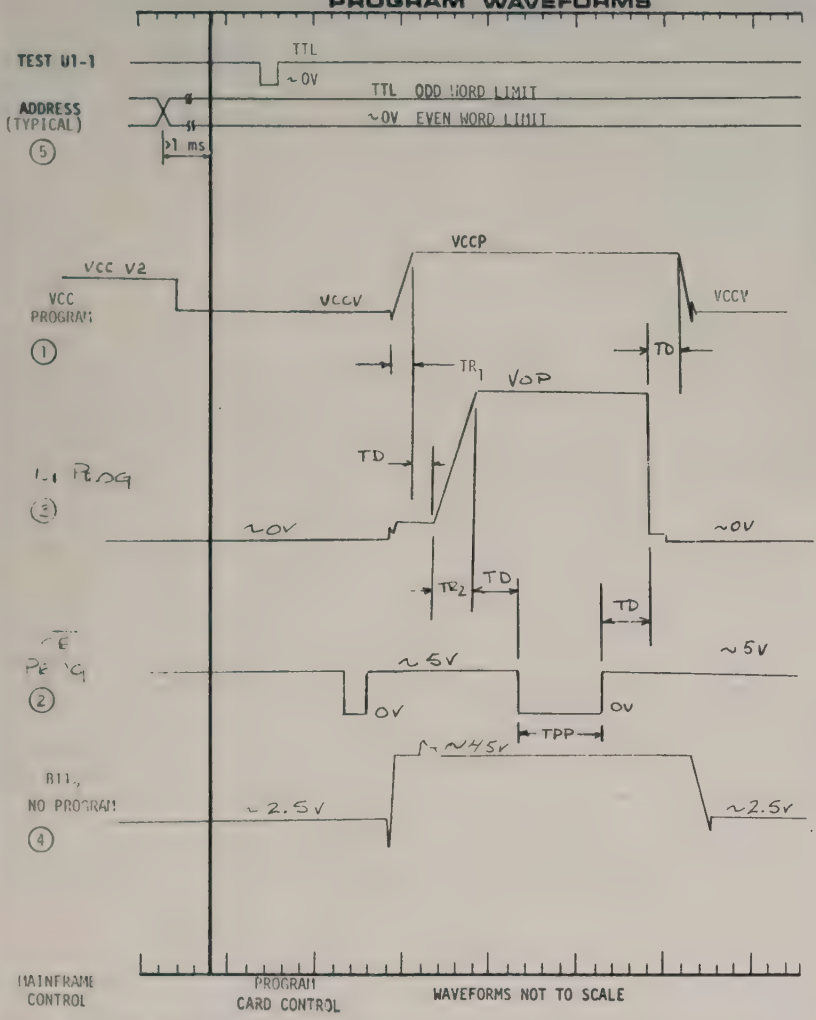
6. Stop programming:

Models 1 – 5 and 9, Press: STOP

System 19, press: KEYBD

			DATE	SYM	REVISION RECORD	DR	CK
	-	CN#22R10					
	G	ECN#2406	8-9-77	D	C.N. #1563	CJ	TI
			8-77	-	ECR #1604 (re-typed)	MW	
			1-23-78	E	C.N. #2056		
			3-13-78	F	ECN#1678		

PROGRAM WAVEFORMS



NOTES

1225
DIGITAL CARD JUMPERS
- JP1 = OPEN
- JP2 = SHORT
- JP3 = SHORT
- JP4 = SHORT
- JP5 = SHORT
- JP6 = SHORT
- JP7C = 1 PULSE REJECT
- JP7M = 1 PULSE REJECT
- JP8 = SHORT
- JP9 = N
- JP10 = WORD LIMIT = 2048

ABORT TIMER = JP1 = NOT USED

PAUSE TIMER (CR2) = OMIT

WAVEFORM VARIABLES

VCCV = 4.5 + 0.1V
VCCP = 8.75 + 0.25V
VOP = 17 + 0.5V
TR_1 = 1 TO 10 u SEC.
TR_2 = 10 TO 50 u SEC.
TPP = 110us ± 10us

VCCV2 = 5.5 + 0.1V
TD > 5 usec

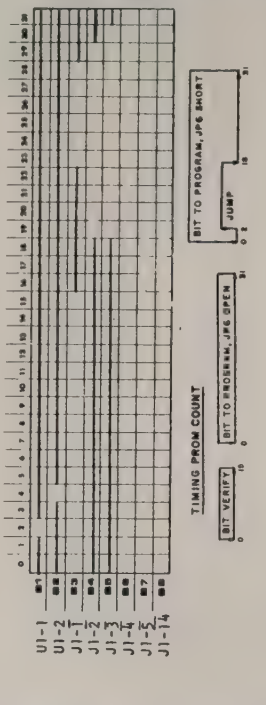
For calibration, the card set polarity defaults to VOH.

These waveforms correspond to callouts on the Calibration Chart. Switch S2 and S3 of the Universal Calibrator to indicated positions to obtain waveforms. Refer to Perfromance Check section of manual for detailed steps.

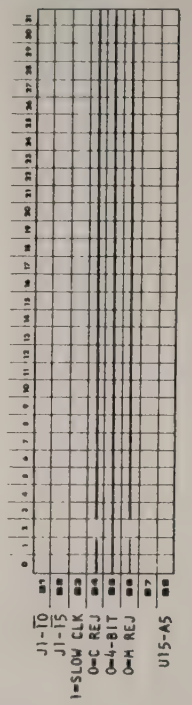
TRUTH TABLES

LINE : HI(1); NO LINE : LOW(Ø)

TIMING FROM U1



MODE FROM U15



DATA I/O ISSAQUAH, WASH.

TITLE: TIMING DIAGRAM	DRAWN BY: K. JONES; APPROVED BY: G.J
SIGNETICS GENERIC	
DATE: 2-25-76	DRAWING NUMBER: 007-1226-2

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4.4.3 REJECT JUMPER REINSTALLATION AND ABORT TEST

Before putting the Program Card Set back in use, it is necessary to reinstall the reject (abort) jumper and confirm the operation of the abort function on the digital card.

1. Turn the programmer power OFF.
2. Remove the digital card from the card slot.
3. Refer to the Timing Diagram for the reject jumper number and make sure to install the jumper in the position from which it was removed.
4. Reinstall the digital card in the card slot.
5. Repeat the key sequence in Waveform Test Procedure, paragraph 4.4.2, steps 1-5.
6. With Universal Calibrator switch positions selected to observe the test pulse waveform, repeat step 6 of the Test Procedure. Note with the oscilloscope that the waveform display is terminated by the programmer. This indicates that the abort function of the digital card is operative.

SECTION 5

CIRCUIT DESCRIPTION

5.1 INTRODUCTION

The Data I/O Program Card Set consists of a digital card, an analog card, and interconnecting cables. Both cards interface with the programmer and with each other. The analog card interfaces with the device being programmed or read. Figure 5-1 gives a generalized block diagram of the relations among the cards, the programmer, and the device.

5.1.1 DIGITAL CARD

The digital card receives data from the programmer on the DI bus, and from the device on the DO bus. The data on these busses are compared at each bit both before and after programming. At each bit, the digital card continues to command program pulses from the analog card until the bit is programmed unless an ABORT or REJECT is signalled.

5.1.2 ANALOG CARD

The analog card receives bit and word addresses, timing and mode commands. In turn, the analog card supplies programming signals of voltages and currents specified by the device manufacturer. When recommended by the manufacturer, each programmed bit is tested for loading and/or leakage. The analog card reads the device, once it is programmed, to verify that programmed data matches truth-table data.

5.1.3 DETAILED CIRCUIT DESCRIPTION

The following paragraphs explain the functions of the digital card and analog card.

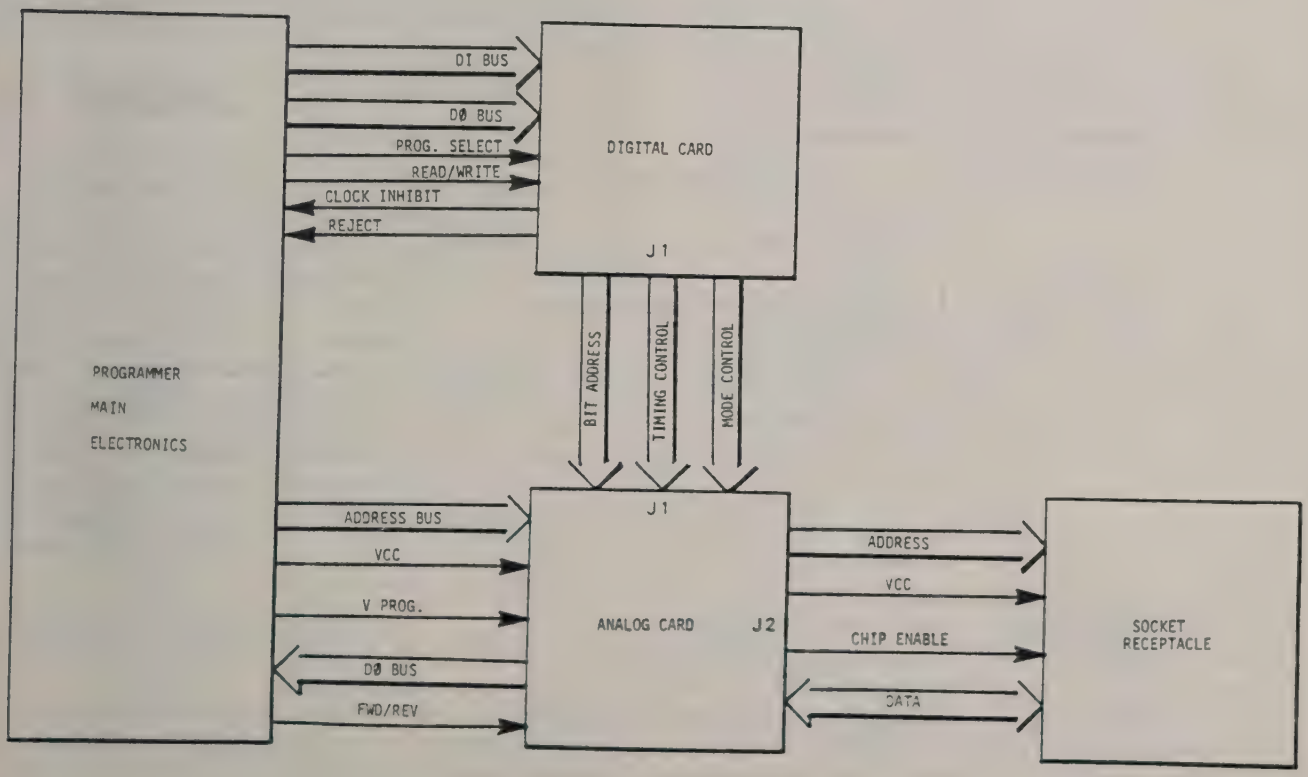


Figure 5–1. Simplified Block Diagram of Program Card Set

5.2 DIGITAL CARD

5.2.1 BLOCK DIAGRAM

Figure 5-2 gives a generalized block diagram of the digital card This diagram shows signal flow and functional relationships between the blocks but does not include detailed interconnect information. Refer to the schematics and timing diagram (with truth tables) for details of circuit connection and operation. The following paragraphs discuss the functions performed by the digital card.

5.2.2 PROGRAM MEMORY

When the digital card is selected for operation, the Program Memory will set upon receiving a Write command on AA. This causes the Clock Generator on the digital card to begin operation and halts the programmer clock. Initialization of the Program Pulse Counter, Bit Counter and Sequence Counter and clearing of the Over-program Counter occur before the Program Memory is set.

5.2.3 CLOCK GENERATOR

When the Program Memory toggles in response to the Write and Program Select commands, the Clock Generator begins operation and the programmer clock is inhibited. Clock pulses increment the Sequence Generator. The clock rate is determined by the Mode and Timing PROM or by High Order Memory (with JP8 connected). The Clock may be halted by the Abort Timer or by the Pause Timer (with CR2 connected).

5.2.4 THE SEQUENCE COUNTER AND TIMING PROM

The Sequence Generator consists of a 4-bit counter which drives the 32x8 Timing PROM. The combination generates timing signals for analog control, along with Bit Test and Bit Increment pulses, which are used on the digital card. (See the Timing Diagram.) A clock pulse is also output for PROMs with registers.

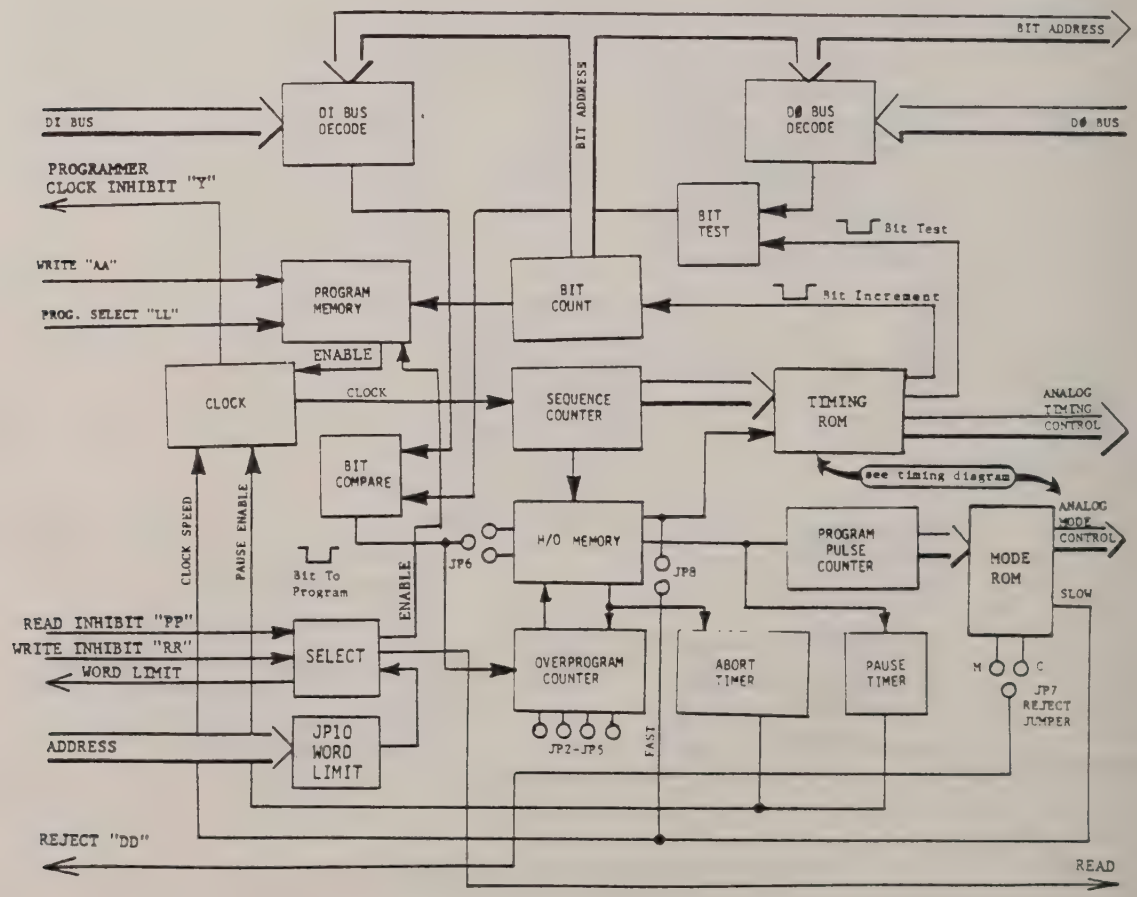


Figure 5–2. Block Diagram, 1225 Digital Card

5.2.5 BIT COUNTER

The Bit Counter counts Bit Increment pulses arriving from the Timing ROM. Bit Increment pulses are counted, however, only when H/O Memory is enabled via a Bit to Program pulse from the Bit Compare gate. The Bit Counter counts down from either 4 or 8, as determined by input from the analog card or from the Mode PROM. Output from the Bit Counter controls the DO Bus Decoder and DI Bus Decoder. When the Bit Counter reaches zero, its borrow output is used to reset the Program Memory.

5.2.6 PROGRAM PULSE COUNT AND MODE CONTROL

As program pulses are delivered to the PROM being programmed, the Program Pulse Counter counts up; outputs from the Program Pulse Counter are used as address line inputs to the Mode Control PROM. The Timing diagram includes the truth table for the Mode Control PROM. Outputs of Mode ROM control the magnitude of program pulses (bits 1 and 2), along with clock speed (bit 3). Bits 4 and 5 control the number of programming attempts allowed before a reject is returned to the programmer; reject jumper JP7 selects either the M line or the C line. (See the Timing Diagram for the pulse numbers selected.)

5.2.7 TIMING PROM

Output words from the Timing PROM are used in the serial Verify and Program operations, as shown in the Timing Diagram. Verify operations use Low Order words 0 to 15; Program operations use High Order words 16 through 31. Words 8 through 11 are used to output control for VCC voltages during Read and Verify operations. These operations occur under machine control when the digital card is not selected. At the beginning of a programming sequence (word 2), the Timing PROM outputs a Bit Test pulse to the Bit Test gate. If the DO Bus Decoder determines that there is no bit already programmed in the PROM, and if the DI Bus Decoder determines that there is a bit to program, then the Compare Gate outputs a Bit to Program pulse.

5.2.8 OVERPROGRAM COUNTER

The Bit to Program pulse arrives at the preset input of the H/O Memory and at the load port of the Overprogram Counter. As H/O Memory is preset, the Bit Count Gate is disabled and remains so until the Overprogram Counter clocks H/O Memory after the bit has been programmed.

At H/O Memory Word 15, the carry pulse from the Sequence Counter, is allowed to toggle U13B. (See Schematic.) As U16B is toggled the fifth address line to the Timing PROM is enabled, and it advances into High Order (Program) Count, words 16 through 31.

At word count 31, the Sequence Counter outputs another carry pulse to H/O Memory. The carry pulse toggles U13B which sets the Timing ROM back to Low Order Count (Verify). At word 2, again, a Bit Test pulse is output from the Timing PROM; if the buses compare at Bit Test (bit is programmed), the output of Bit Compare gate remains unchanged (no Bit to Program), the H/O Memory remains enabled, and the Bit Count gate remains disabled.

At word 15 the Sequence Counter outputs another carry pulse which again causes a High Order (Program) count, causing the Overprogram Counter to decrement. The above cycle repeats until the Overprogram Counter outputs a borrow pulse after counting down from the level preset by JP2–JP5. The borrow pulse clocks H/O Memory which enables the Bit Count gate, allowing it to decrement the Bit Count to the next bit.

Some digital cards are wired with JP6 shorted. If JP6 is shorted Program Memory holds H/O Memory reset so that the Timing PROM jumps to High Order (Program Cycle) after Bit Test. When a Bit to Program pulse is received at (shorted) JP6, the fifth address input line to the Timing PROM goes high and H/O Memory is enabled. At Word 31, the carry pulse from the Sequence Counter shifts the count sequence back to Low Order. With JP6 shorted, the total sequence is 16 clock pulses long.

5.2.9 ABORT TIMER

The Abort Timer measures the time required to program a bit. If programming time is excessive, and JP1 is shorted, a REJECT is signaled and the clock is halted. The Abort Timer is connected to the Overprogram Counter such that an abort is possible only during Low Order count (Verify cycle).

5.2.10 PAUSE TIMER

The Pause Timer measures the time to program the PROM. A transistor is used in conjuction with the timing components to integrate out the time that the Program Memory is set. If programming time exceeds the value set by circuit components, the Clock is stopped in order to allow the PROM to cool; after a pause in the order of seconds the Clock is allowed to start again, and programming continues. Pause Timer output is gated with the Timing PROM so that a pause cannot occur during program pulses.

5.2.11 SELECT GATES

U17 and U18 (on schematic) monitor Program Select (LL), Write Inhibit (PP), Read (X), and Read Inhibit (RR) in order to enable operation of the digital card. Output from Read Gate U17 is routed to the analog card to control the Data Bus Drivers.

5.2.12 WORD LIMIT SELECT

Word Limit is jumper—selected at JP10 on the digital card to 32, 64, 256, 512, 1024, or 2048. JP10 limits the address range of the programmer through the Word Limit line (CC), according to the configuration of the PROM being programmed.

5.3 ANALOG CARD

5.3.1 BLOCK DIAGRAM

Refer to Figure 5—3 for functions and signal flow of the analog card.

5.3.2 BIT DECODE

PROM bits are programmed individually within a given PROM work. Bit information in BCD form arrives at analog card J1 and is used to drive the BCD to decimal Bit Decoder. Decoder outputs enable appropriate Bit Program Switches to transfer program pulses to the bit lines of the PROM being programmed.

During clock periods 21—24 of the program cycle the Bit Switches are turned ON, allowing the output of the Program Voltage Generator to reach the PROM bit lines.

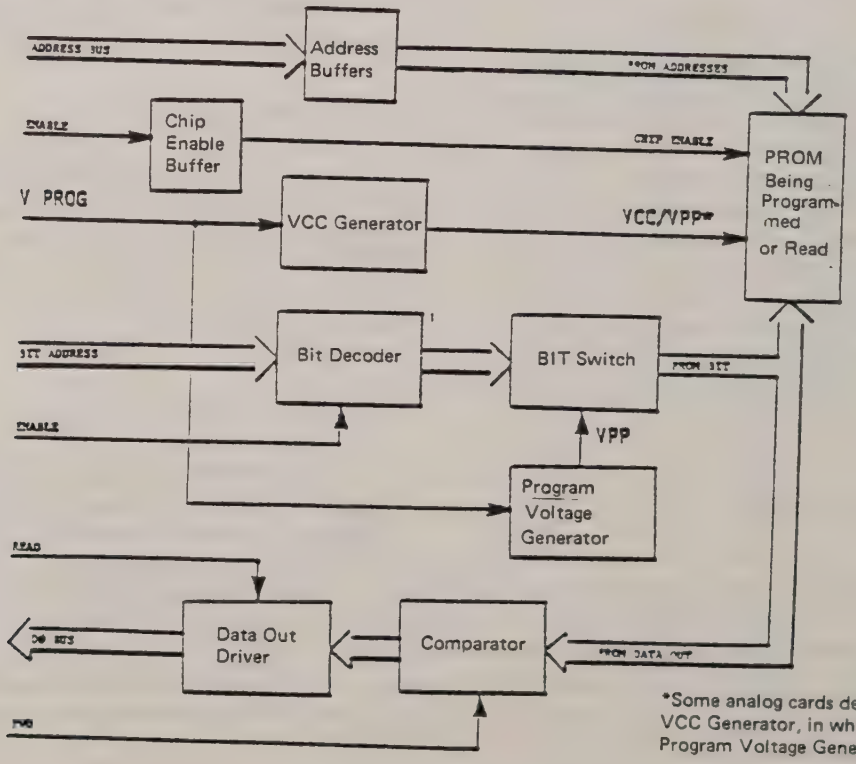
5.3.3 PROGRAM VOLTAGE GENERATOR

During the initial portion of the program cycle (period 18) the Program Voltage Generator is switched ON. The Program Voltage Generator output is routed to the PROM.

The Program Voltage Generator receives voltage increment inputs from the digital card Mode Control PROM. As the programmer attempts to program the PROM, increasingly higher program voltages are used. (See the Timing Diagram.) The magnitude of Program voltages (High and Low) are set by calibration resistors.

5.3.4 RAMP GENERATOR

The Ramp Generator consists of a current limiter and an emitter follower. The emitter follower provides voltage to the Bit Switches during clock periods 21—24, allowing output from the Program Voltage Generator to reach the PROM bit being programmed.



*Some analog cards derive VPP from the VCC Generator, in which case the VPP Program Voltage Generator may be omitted.

Figure 5—3. Block Diagram, 1226—1 Analog Card

5.3.5 VCC GENERATOR

The VCC Generator outputs three voltages; VCC Program, VCC low, and VCC High. During the program cycle, VCC is set at VCC Program, as determined by the setting of a calibration resistor. When the programmer is in FWD, VCC is nominally set at VCC Low, as determined by another calibration resistor. With the programmer in REV, VCC Generator output is at VCC High. Refer to the Timing Diagram for details on voltage levels; see Calibration section for adjustment information.

5.3.6 COMPARATORS

PROM output is tested during Verify and Read for VOL in FWD and for VOH in REV. In FWD, a load switch connects load resistors to PROM output bits. Current through these resistors develop voltages at the + inputs of the comparators. Positive input is compared with negative input from a reference level generator. If the levels compare (bit is programmed) the information is transferred to the digital card through the DO Bus.

In REV, the situation is similar, but PROM VOH levels are tested, and the reference level generator outputs a higher voltage to the negative inputs of the Comparator.

Warranty

Data I/O equipment is guaranteed against defects in materials and workmanship. The warranty period is ninety days on new equipment, and thirty days on used equipment. Warranty period begins on receipt of equipment. Data I/O will repair or replace, at Data I/O's option, any equipment found to be defective within the warranty period.

Warranty service will be provided by Data I/O within a reasonable amount of time after notification by the purchaser to Data I/O of equipment malfunction. This service shall not apply to equipment that has been subjected to abuse, misuse, negligence or accident as determined by Data I/O, or to which any modifications, alterations, or attachments have been made without written authorization from Data I/O, nor shall it apply if the equipment is installed or operated in an environment containing excessive dirt, dust, moisture, fumes, humidity, or extremes of temperature.

This warranty policy is in lieu of all other warranties, expressed or implied, unless standard warranty exceptions are granted by Data I/O in writing.

Service

After expiration of the warranty period, service and repairs are billed at standard hourly rates, plus expenses, portal-to-portal. Time and one-half rate will apply outside of normal working hours.

Cost of engineering (where applicable) and parts, plus the cost of installation is billed at standard service labor rates when implementing approved, customer requested modifications.

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Products returned to Data I/O should be accompanied by a letter or enclosure explaining the reason for their return and action requested of Data I/O. Please include the following additional information: Company name and address; attention of; method of shipment desired; serial number; date of purchase; billing information, and purchase order number.

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Issaquah, Washington 98027

From Europe:

DATA I/O EUROPE
Vondelstraat 50-52
Amsterdam, Netherlands

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e. Shipping address of firm, including zip code.
f. Full name of person ordering the part(s).
g. To whose attention the part(s) are to be shipped.
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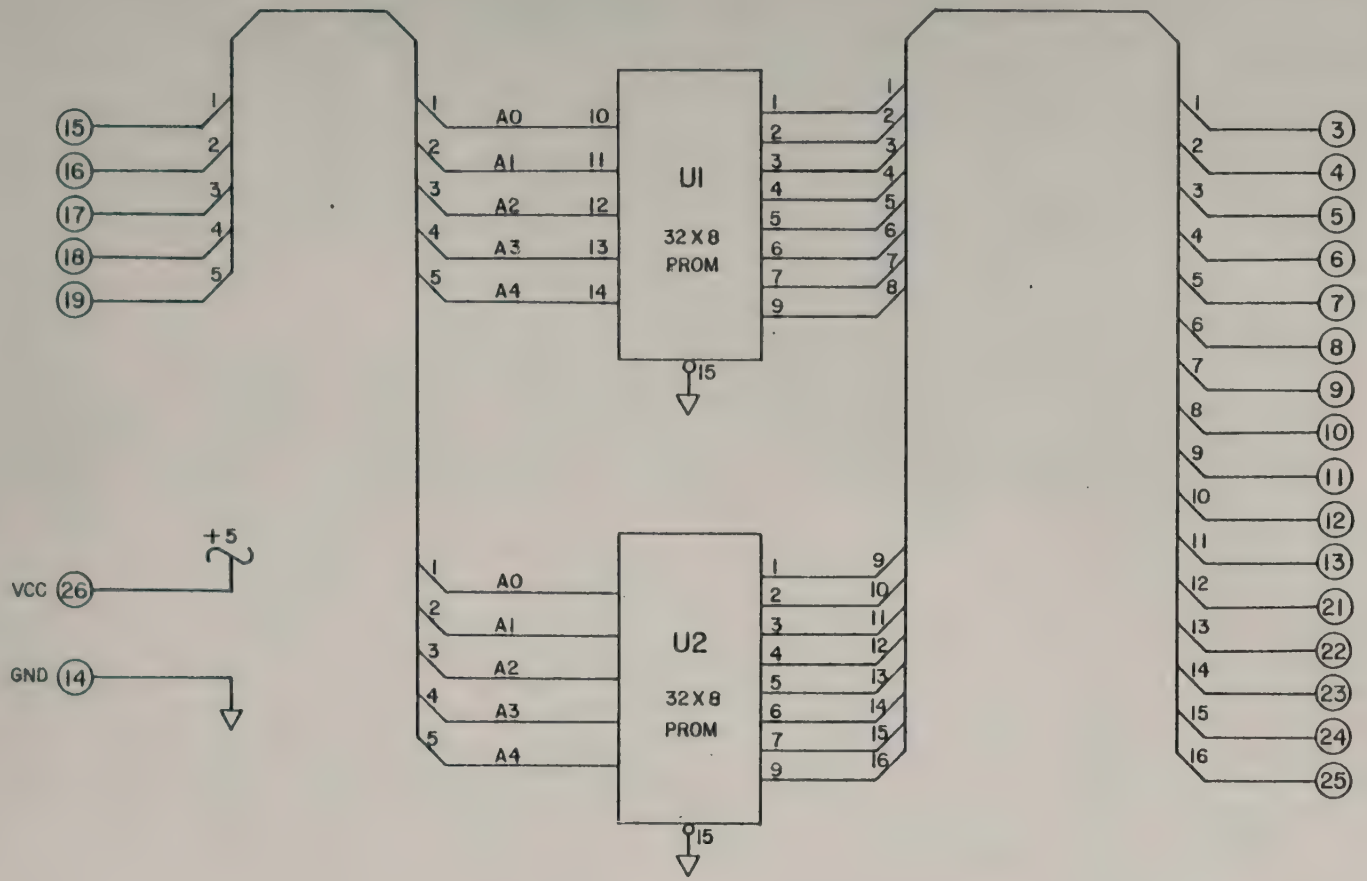
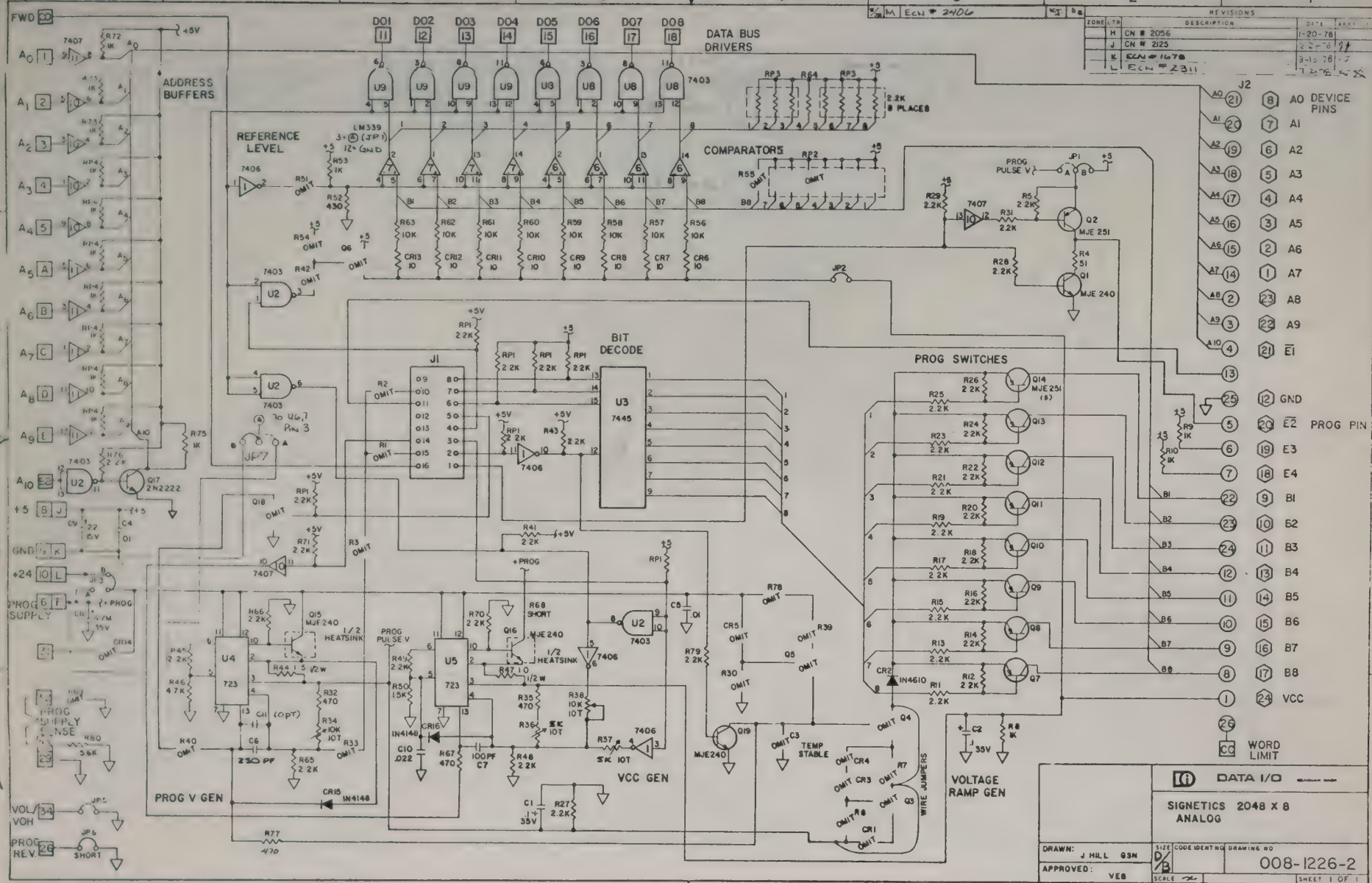
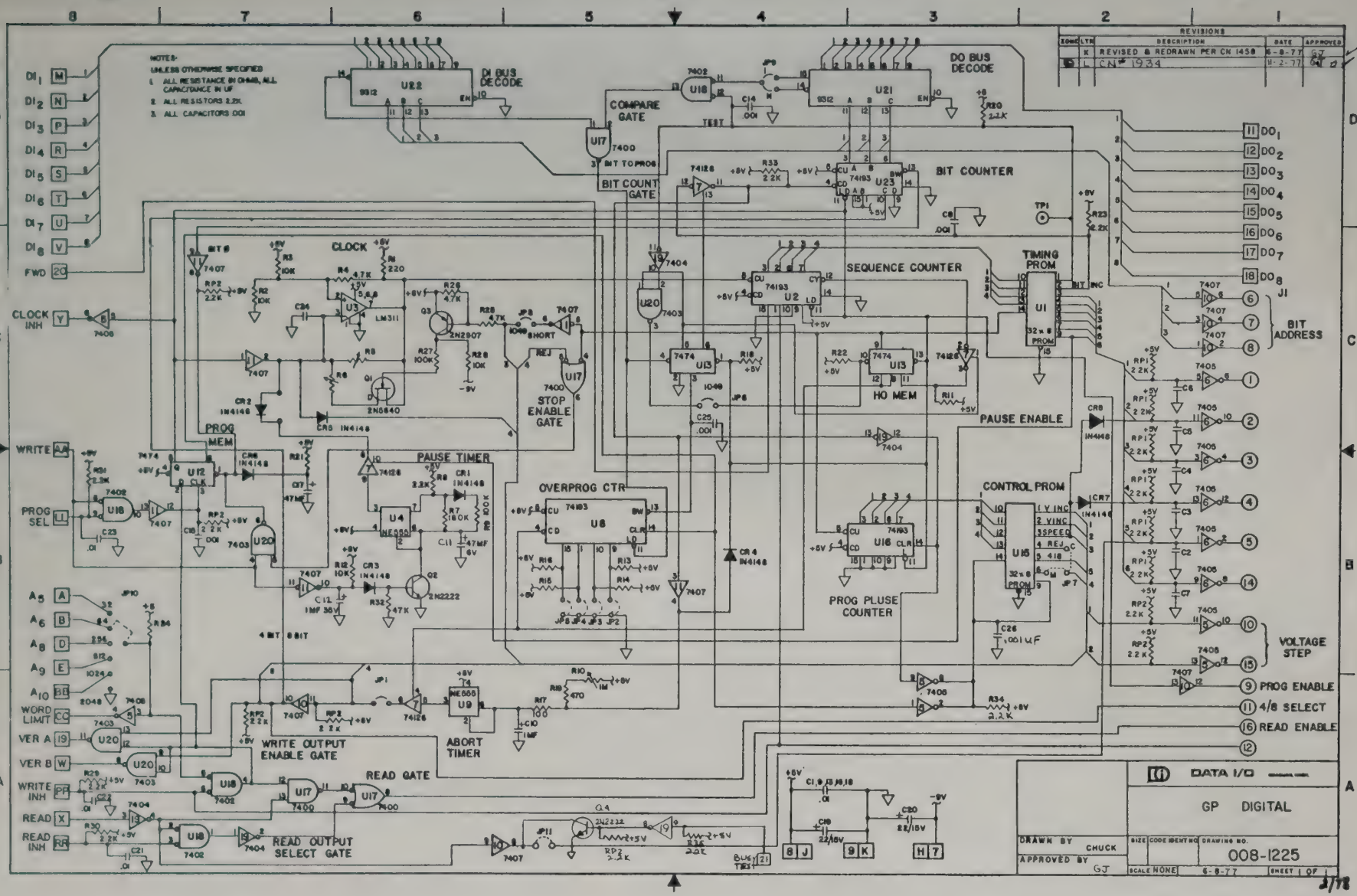
11-19-76	A	RELEASE		



TOLERANCES (EXCEPT AS NOTED)	DATA I/O ISSAQUAH, WASH		
DECIMAL ±		SCALE	DRAWN BY G. ROPPE
FRACTIONAL ±	TITLE PLUG IN ADAPTER (UNIVERSAL CALIBRATOR)		APPROVED BY [illegible]
ANGULAR ±	DATE 10-15-75	DRAWING NUMBER 008-1072	


DATA BUS DRIVERS
ADDRESS BUFFERS
REFERENCE LEVEL
COMPARATORS
BIT DECODE
PROG SWITCHES
PROG V GEN
VCC GEN
VOLTAGE RAMP GEN
PROG SUPPLY
PROG SUPPLY SENSE
WIRE JUMPERS
J2
A0 DEVICE PINS
PROG PIN
WORD LIMIT
DATA I/O
SIGNETICS 2048 X 8
ANALOG
DRAWN: J HILL GSN
APPROVED: VEB
008-1226-2
SHEET 1 OF 1


NOTES:
UNLESS OTHERWISE SPECIFIED
1. ALL RESISTANCE IN OHMS, ALL CAPACITANCE IN UF
2. ALL RESISTORS 2.2K
3. ALL CAPACITORS .001
REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
K | REVISED & REDRAWN PER CN 1458 | 6-8-77 | BT
L | CN# 1934 | 11-2-77 | BT
DI BUS DECODE
DO BUS DECODE
COMPARE GATE
BIT COUNT GATE
BIT COUNTER
SEQUENCE COUNTER
TIMING PROM
CLOCK
PROG MEM
PAUSE TIMER
OVERPROG CTR
HO MEM
PAUSE ENABLE
CONTROL PROM
PROG PLUSE COUNTER
STOP ENABLE GATE
WRITE OUTPUT ENABLE GATE
ABORT TIMER
READ GATE
READ OUTPUT SELECT GATE
BIT ADDRESS
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4/8 SELECT
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DATA I/O
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